

SR mosfet parameters FDD86250_F085

C_{iss} [F]	1.90E-09	Input capacitance
R_{gFET} [Ω]	0.5	Gate resistance
Q_g [C]	37.00E-09	Total gate charge (max.)
Q_{gd} [C]	7.00E-09	Gate to drain (Miller) charge
Q_{gs} [C]	11.00E-09	Gate to source charge
V_{gs} [V]	10	Gate to source voltage
V_m [V]	5.5	Gate plateau voltage
V_F [V]	1.2	Body diode forward voltage drop (max.)

CF-DIC parameters

$f_{sw, max}$ [Hz]	31,000	Push-pull switching frequency
Gate trace length [mm]	12	
L_g [H]	12.00E-09	Trace loop inductance (1 nH/mm)
$T_{IC, amb}$ [$^{\circ}C$]	50	Ambient temperature (i.e. PCB temperature)
V_{cc}	6.5	Supply voltage
I_{out} [A]	5	Max. Output current

IR11688 parameters

R_{up} [Ω]	6	Pull up resistance
R_{down} [Ω]	1.5	Pull down resistance
I_{QCC} [A]	500.00E-06	Quiescent current (max.)
$V_{g, high}$ [V]	11.9	Gate high voltage, typical
T_{b1} [s]	250.00E-09	Approx. equal to T_{Don}

Minimum recommended gate resistor

$R_{g, loop} > 2 * \text{sqrt}(L_g / C_{iss})$	5.0
$R_g = R_{g, loop} - R_{gFET} - R_{down}$	3.0
R_g [Ω]	Selected resistor
	3.3

Gate resistor and IC power loss calculation

$C_{sync} = (Q_g - Q_{gd} - Q_{gs}) / (V_{gs} - V_m)$	4.22E-09	4.22 nF
$I_{cc} = I_{QCC} + 2 * f_{sw, max} * C_{sync} * V_{cc} + (0.285 * V_{cc} - 0.425) * 1E-9 * f_{sw, max}$	2.25E-03	2.25 mA
$P_{dr} = C_{sync} * V_{cc}^2 * F_{sw, max}$	5.53E-03	5.53 mW
$R_{sink} = 2 * R_{down}$	3	
$R_{source} = 2 * R_{up}$	12	
$P_{Rgext} = [(R_g + R_{gFET}) / (R_g + R_{gFET} + R_{source}) + (R_g + R_{gFET}) / (R_g + R_{gFET} + R_{sink})] * P_{dr} / 2$	2.21E-03	2.21 mW
$P_{IC} = V_{cc} * I_{cc} - 2 * P_{Rgext}$	10.18E-03	10.18 mW

SR MOSFET power loss calculation

$I_{SPK} = P_i / 2 * I_{out}$	7.85E+00	
$I_{S1} = I_{SPK} * \sin(2 * \pi * f_{sw, max} * T_{b1})$	382.30E-03	
$P_{body1} = 1 / 2 * T_{b1} * f_{sw, max} * V_F * I_{S1}$	1.78E-03	1.78 mW

Supply voltage filtering

Δ_{vcc} [V]	0.1	Acceptable ripple
R_{cc} [Ω]	10	Selected resistor
$C_{dc, min} = I_{cc} / (f_{sw, min}) * \Delta_{vcc}$	7.24454E-07	0.72 μF